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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/582,377	03/29/2007	Stanton Earl Weaver Jr.	GLOZ 200196US01	3872

27885 7590 12/28/2010

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EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2895	

MAIL DATE	DELIVERY MODE
12/28/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,377	WEAVER JR. ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/22/2010, 6/29/2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31 and 38-41* is/are pending in the application.

4a) Of the above claim(s) *7-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15-31 and 38-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Election/Restriction

Applicant's election with traverse of 1-6, 15-31, 38-41 in the reply filed on Oct. 22, 2010 is acknowledged. The traversal is on the ground(s) that the restriction does not allege that examination of all claims would impose a serious burden and does not meet the threshold of requirement for a restriction. This is not found persuasive because there is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 15-26, 28-31 and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. 6,674,159 in view of Kropp 2004/0136658.

The reference(s) teach the features:

Peterson discloses a light emitting package comprising:

a chip carrier 16 or 81 having top and bottom principal surfaces, figs. 11D-12B, 14A-14C,18-19,

at least one light emitting chip 100 attached to the top principal surface of the chip carrier 16 or 81,

a lead flame 24 attached to the top principal surface of the chip carrier 16 but not to the bottom principal surface of the chip carrier, fig. 11D-12B, 14A-14C, 18-19, and see fig. 3 of Kropp: lead frame 51, 52, carrier 4, printed circuit board 6.

Regarding claim 2. The light emitting package as set forth in claim I, further comprising:

an encapsulant encapsulating 128, 129 at least the light emitting chip and the top principal surface of the chip carrier, the bottom principal surface of the chip carrier and leads of the lead frame extending outside the encapsulant, figs. 11D-12B, 18-19.

Regarding claim 3. The light emitting package as set forth in claim 1, further comprising:

one or more areas of electrically conductive material disposed on the top principal surface of the chip career, the attachment of the lead frame to the top principal surface electrically contacting the one or more areas of electrically conductive material 24, figs. 11D-12B, 18-19.

Regarding claim 4. The light emitting package as set forrth in claim 3, wherein the one or more areas of electrically conductive material include:

a first area of electrically conductive material 24 defining a first electrical terminal;

a second area of electrically conductive material 24 electrically isolated from the first area, the second area defining a second electrical terminal of opposite electrical polarity from the first electrical terminal;

electrodes of the light emitting chip being electrically connected with the first and second electrical terminals; and

the lead frame 24 being attached to the first and second electrical terminals, figs. 11D-12B, 14A-14C, 18-19.

Regarding claim 5. The light emitting package as set forth in claim 4, wherein the light emitting chip 100 is flip-chip bonded to the first and second electrical terminals, figs. 11D-12B, 14A-14C, 18-19.

Regarding claim 6. The light emitting package as set forth in claim 4, wherein the light emitting chip is flip-chip bonded to the first and second electrical terminals using one of thermosonic bonding, solder, and a conductive epoxy, col. 2, lines 50-67.

Regarding claim 15. The light emitting package as set forth in claim 1, wherein the light emitting chip receives electrical power through the lead frame and does not receive electrical power through the bottom principal surface of the chip carrier figs. 11D-12B, 14A-14C, 18-19.

Regarding claim 16. The light emitting package as set forth in claim 1, wherein the bottom principal surface of the chip carrier is electrically isolated from the lead frame, figs. 11D-12B, 14A-14C, 18-19.

Regarding claim 17. The light emitting package as set forth in claim 1, wherein the lead frame 24 has electrical leads extending from portions of the lead frame attached to the top principal surface of the chip career, the electrical leads being shaped to include lead portions 702 approximately coplanar with the bottom principal surface of the chip carrier, figs. 15C, 19.

Regarding claim 18. The light emitting as set forth in claim 17, wherein the bottom principal surface of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame, fig. 21

Regarding claim 19. The light emitting package as set forth in claim 18, wherein the chip carrier, light emitting chip, and lead frame define a surface mountable unit, the light emitting package further comprising:

printed circuitry 402, the surface mountable unit being mounted on the printed circuitry with the lead portions approximately coplanar with the bottom principal surface of the chip carrier electrically contacting the printed circuitry, figs. 18-19.

Regarding claim 20. The light emitting package as set forth in claim 19, further comprising:

a printed circuit board 402 including the printed circuitry, the bottom principal surface of the chip carrier being in thermal contact with the printed circuit board, figs. 18-19.

Regarding claim 21. A light emitting package comprising:

a chip carrier 16 or 81 having top and bottom principal surfaces, figs. 11D-12B, 14A-14C,18-19,

at least one light emitting chip 100 attached to the top principal surface of the chip carrier 16 or 81,

a lead frame 24 attached to the top principal surface of the chip carrier, the lead frame having electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions 702 approximately coplanar with the bottom principal surface of the chip carrier, figs. 15C, 19, and see fig. 3 of Kropp: LED 1, lead frame 51, 52, carrier 4, printed circuit board 6,

wherein the bottom principal surface of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame and the chip carrier, light emitting chip, fig. 21,

lead frame define a surface mountable unit, figs. 11D-12B, 14A-14C,18-19,

a printed circuit board 402 on which the printed circuitry is disposed, the surface mountable unit being mounted on the printed circuitry with the lead portions 702 approximately coplanar with the bottom principal surface of the chip carrier electrically contacting the printed circuitry, the bottom principal surface of the chip carrier being in direct contact with the printed circuit board, fig. 15C, 19.

Regarding claim 22. The light emitting package as set forth in claim 21, wherein the chip carrier is soldered to the printed circuit board 402, figs. 18-19.

Regarding claim 23. The light emitting package as set forth in claim 21, wherein the chip carrier is soldered to the printed circuit board, said soldered connection being thermally conductive but not conducting electrical current when the light emitting chip is operated, col. 28, lines 25-35.

Regarding claim 24. The light emitting package as set forth in claim 21, wherein an attachment between the lead portions contacting the printed circuitry is different from an attachment of the bottom principal surface of the chip carrier contacting the printed circuit board, figs. 18-19.

Regarding claim 25. The light emitting package as set forth in claim 21, further comprising:

an encapsulant 128, 129 encapsulating at least the light emitting chip and the top principal surface of the chip carrier, the bottom principal surface of the chip carrier and at least the lead portions approximately coplanar with the bottom principal surface of the chip carrier extending outside the encapsulant, figs. 11D-12B, 14-19.

Regarding claim 26. The light emitting package as set forth in claim 1, wherein the chip carrier comprises: a semi-insulating silicon wafer, col. 11, lines 25-67.

Regarding claim 27, The light emitting package as set forth in claim 1, wherein the chip career comprises:

electrically conductive silicon having at least the top principal surface coated with an insulating layer, col. 11, lines 25-67, and see para. 35, figs 1-9 of Kropp..

Regarding claim 28. The light emitting package as set forth in claim 1, wherein the chip career comprises:

metal having at least the top principal surface coated with an insulating layer, col. 11, lines 25-67.

Regarding claim 29. The light emitting package as set forth in claim 1, wherein the chip carrier comprises: thermally conductive plastic, col. 8, lines 26-67, col. 11, lines 26-67.

Regarding claim 30. The light emitting package as set forth in claim 1, wherein the chip career comprises: ceramic, col. 11, lines 26-67.

Regarding claim 31. The light emitting package as set forth in claim 1, wherein the chip carrier is electrically insulating and the lead frame is electrically conductive, col. 11, lines 26-67.

Regarding claim 38. The light emitting package as set forth in claim 1, wherein the lead frame includes electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions distal from the chip carrier that are approximately coplanar with the bottom principal surface of the chip carrier, figs. 11D-19.

Regarding claim 39. A light emitting package comprising:

a chip carrier 16 or 81 having top and bottom principal surfaces, figs. 11D-12B, 14A-14C,18-19,

at least one light emitting chip 100 attached to the top principal surface of the chip carrier 16 or 81,

a lead frame 24 attached to the top principal surface of the chip carrier, the lead frame having electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions 702 approximately coplanar with the bottom principal surface of the chip carrier, figs. 15C, 19, and see fig. 3 of Kropp: LED 1, lead frame 51, 52, carrier 4, printed circuit board 6.

Regarding claim 40. The light emitting package as set forth in claim 1, further comprising: solder bonds attaching the lead frame to the top principal surface of the chip career, figs. 11D-19.

Regarding claim 41. The light emitting package as set forth in claim 39, further comprising: solder bonds attaching the lead frame to the top principal surface of the chip carrier, figs. 11D-19.

The difference between the reference(s) and the claims are as follows: Peterson teaches a light emitting package having a lead frame 24 connected to the top surface of carrier. Kropp teaches at para. 35 and figs. 1-9, a light emitting package having a lead frame 51, 52 connected to the top surface of silicon carrier/substrate 4.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Peterson's device with a lead frame connected to the top surface of silicon carrier/substrate as suggested by Kropp so that light can transmit through the silicon carrier/substrate.

Claim 27 is rejected under 35 U.S.C 103 as being unpatentable over Peterson in view of Kropp as applied to claims 1-6, 15-26, 28-31 and 38-41 above, and further in view of Cunningham et al. 6,005,262.

The difference between the references applied above and the instant claim(s) is: Peterson in view of Kropp teaches a silicon carrier. However, Cunningham et al. teaches at fig. 3, an insulating layer 148 formed on the silicon carrier 214.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings having an insulating layer formed on the silicon carrier as taught by Cunningham et al. so that bonding pads can be formed on the top surface of silicon carrier.

Conclusions

Applicant's arguments filed Oct. 22, 2010 and June 29, 2010 have been fully considered but they are not persuasive. Because the newly cited references teaches a lead flame attached to the top principal surface of the chip carrier but not to the bottom principal surface of the chip carrier as set forth above.

Peterson teaches a light emitting package having a lead frame connection to the carrier, Kropp teaches a light emitting package having a lead frame connection to the silicon carrier, and Cunningham teaches a light emitting package having a lead frame connection to the insulated silicon carrier, hence the combination of Peterson, Kropp and Cunningham is proper. Therefore, it is clearly that the combination of Peterson, Kropp and Cunningham meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of “a person of ordinary skill can implement a predictable variation, §103

likely bars its patentability". And, it is also clearly that the combination of Peterson, Kropp and Cunningham meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of "If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103". Also see MPEP §2143.

It is common sense that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle. See KSR international v. Teleflex, US Supreme Court, 127 S.Ct. 1727 (2007). And, see Ball Aerosol v. Limited Brands, Inc., 555 F.3rd 984, 89 U.S.P.Q. 2d 1870 (Fed Cir. 2009). Boston Scientific Scimed, Inc. v. Cordis Corp., 554 F.3d 982, 89 U.S.P.Q. 2d, 1704 (Fed. Cir. 2009).

More details of U.S. Supreme Court in KSR international v. Teleflex, US Supreme Court, 127 S. Ct. 1742, 82 USPQ 2d at 1390. Granting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103.

When a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, §103 likely bars its patentability. Moreover, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill.

It is common sense that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle. See KSR international v. Teleflex, US Supreme Court, 127 S.Ct. 1727 (2007).

In *Sakraida* v. *AG Pro, Inc.*, 425 U. S. 273(1976), the Court derived from the precedents the conclusion that when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious. *Id.*, at 282. The principles underlying these cases are instructive when the question is whether a patent claiming the combination of elements of prior art is obvious. When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary

skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from: Monday: 7:00 am-4:00 pm; Tuesday: 7:00am- 4:00pm; Friday: 7:00 am-11:00am. Tuesday & Wednesday are off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, 571-272-1736.

The fax phone number for this Group is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/H.Jey Tsai/
Primary Examiner, Art Unit 2895
12/22/2010